San Francisco State University

School of Engineering

ENGR 852: Advanced Digital Design (3 units)

Course Objective:

This course is designed to teach students advanced topics in digital design, from high level system description down to ASIC implementation. The course begins with a review of the digital design flow and fundamentals of digital design and then moves towards the system level design of digital systems.

The design at the system level is done using Verilog hard-ware description language. The students will experience HDL description of digital systems, synthesis, and optimization to gate-level.

The main objectives of the course is

- To prepare the student to be an entry-level industrial standard cell ASIC or FPGA designer.
- To give the student an understanding of issues and tools related to ASIC/FPGA design and implementation including timing, performance and power optimization, verification and manufacturing test.

Specific Learning Outcomes:

Students completing the course successfully will

- explain a modern digital design flow
- describe a digital system in Verilog HDL
- perform design optimization and synthesis to gate-level
- use model EDA (Electronic Design Automation) tools for simulation, verification, and synthesis of digital design
- perform post-synthesis design validation
- implement complex digital systems from high-level HDL description down to ASIC implementation

Prerequisites:

- For undergrads, grade of C- or better in ENGR 356 or equivalent
- Basic knowledge of digital design, including combinational logic gates, sequential logic gates, timing design, finite state machine, etc.
- Familiarity with HDL preferred, but not required

ENGR 852 Fall 2013

Instructor:	Xiaorong Zhang, Ph.D.
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Office Hours:	T,Th: 3:00-4:30 pm or by appointment
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Course Website:	https://ilearn.sfsu.edu

(All lecture slides, supplementary materials, and assignments are posted on iLearn.)

Reference Materials:

Purchase is optional.
Main

1. M.D. Ciletti, “Advanced Digital Design with the Verilog HDL (2nd Edition),” (Prentice Hall), 2010. ISBN 0136019285.
2. D.R. Smith and P.D. Franzon, "Verilog Styles for Synthesis," (Pearson Education [Prentice Hall]), 2000.ISBN. 0201618605.

Additional

1. Thomas and Moorby, ``The Verilog Hardware Description Language", 3rd edition, Kluwer Academic. ISBN 0-7923-9723-1.
2. S. Sutherland, S. Davidman, P. Flake, “System Verilog for Design” (Kluwer), 2004, ISBN 1-4020-7350-8.
3. H. Bhatnagar, “Advanced ASIC Chip Synthesis Using Synopsys Design Compiler, Physical Compiler, and PrimeTime”, ISBN 0-7923-7644-7.

Class Schedule

ENGR 852: Monday 6:10pm-8:55pm
Location: TH 210

Topics:

- Introduction to ASIC design
- Review of combinational and sequential logic design fundamentals
- Timing design
- Design of digital hardware using Verilog HDL
- Design of complex systems
- Hierarchy and Partitioning
- Finite State Machines
- Test benches and verification
- Low power design
- Design for test
- Introduction to FPGAs

Tentative Weekly Schedule

Week	Date	Topics	Due
1	8/26	Course overview; Introduction to ASIC Design	
2	9/2	No Class (Labor Day)	
3	9/9	Review of combinational and sequential logic design;	
4	9/16	Timing Design;	Homework 1
5	9/23	Design of digital hardware using Verilog HDL I	
6	9/30	Design of digital hardware using	

		Verilog HDL II	
7	10/7	TBD	
8	10/14	TBD	
9	10/21	TBD	
10	10/28	TBD	Midterm exam (first half of the class meeting)
11	11/4	TBD	Preliminary project report
12	11/11	No class (Veteran's Day)	
13	11/18	TBD	
14	11/25	Fall semester break	
15	12/2	TBD	
16	12/9	TBD	
17	12/16		Oral project presentation
17	12/21		Final Exam
18	12/23		Final project report

Note: This schedule is to be completed and subject to change based on the "reality" of the class performance. Information given in class supersedes this schedule.

Important Dates

Last day to add/drop: Sept. 9, 2013
Last day to withdraw: Nov. 22, 2013
(Please read the last page of the syllabus for more information)

Grading Policy:

Grades will be based on total points earned through the following activities:

Homework	20%
Midterm Exam	15%
Project	40%
Final Exam	25%
Total	100%

Important Dates:

- Preliminary project report due: Mon Nov 4th
- Midterm exam: Mon Oct 28th (first half of the class meeting)
- Oral project presentation: Mon Dec 16th
- Final exam: Sat Dec 21st, 6:10pm-8:55pm, TH 210
- Final project report due: Mon Dec 23th

Notes on grading:

- Both the midterm and the final exams will be comprehensive, open-book, open-notes exams. You may NOT use computers, mobile phones, or PDAs during the exams. Generally, there will be **no make-up exam and no incomplete** grades given. If you miss

an exam, you must notify the instructor before the exam or, if physically impossible, soon after. If you have an acceptable, documented excuse, you may be given a make-up exam. If you do not have an acceptable reason for missing the exam, you will receive zero points for the exam.

- Though you can collaborate during homeworks, **direct copying of solutions, in part or in whole, is not permitted. All code required for the homeworks should be individually designed and developed**.
- A fixed project will be published in the class. The project will be done by the students in pairs. You will be evaluated as a pair.

Policies on Plagiarism

Plagiarism is defined as using someone else's ideas or work as one's own without giving proper credit to the source. The source include public (books, journals, magazines, newspapers, internet, etc.) as well as private (unpublished reports, internal documents, personal work, etc.) materials. The instructor will not accept excuses such as "I forgot to give credit to …," "It's an oversight," or "It's a clerical error."

Students are solely responsible for materials submitted for the course so "My roommate must have done that without my knowledge" is not an acceptable excuse either. That is, no excuses will be accepted if plagiarism is discovered. If a submitted work is found to contain plagiarized material, the work will receive zero credit and the student may be reported to the Student Judiciary Affairs for disciplinary actions. Cheating on tests will also be reported to the Student Judiciary Affairs. Disciplinary actions may include disqualification from the university.

Disability Policy Statement

Students with disabilities who need reasonable accommodations are encouraged to contact the instructor.

The Disability Programs and Resource Center (DPRC) is available to facilitate the reasonable accommodations process. The DPRC is located in the Student Service Building and can be reached by telephone (voice/TTY 415-338-2472) or by email (dprc@sfsu.edu).

(http://www.sfsu.edu/~dprc/facultyfaq.html#1)

Policy on observance of religious holidays

If a student wishes to observe religious holidays and such observances require the student to be absent from class activities, it is the responsibility of the student to inform the instructor, in writing, about such holidays during the first two weeks of the class each semester. If such holidays occur during the first two weeks of the semester, the student must notify the instructor, in writing, at least three days before the date that he/she will be absent.